* 1. OHDB – Hardware ICD

1. OHDB – Hardware ICD
   1. Interface Control Document   
       for the Stratasys Heads Driver Board
2. March 2014

|  |  |  |  |
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1. List of Abbreviations and Acronyms

|  |  |  |
| --- | --- | --- |
| OHDB | - | Objet Heads Driver Board |
| ICD | - | Interface Control Document |
| TBD | - | To Be Defined |

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# Scope

This document describes the OHDB hardware interface to be used by the OHDB software.

# General Description

The Objet Heads Driver Board (OHDB) is one of the electronic boards that comprise the electronics of the Keshet 3D printer.  
The OHDB roles are:

* Control the heat of the Keshet printer printing heads
* Control the heat of the Keshet printer surrounding block of the Keshet heads
* Control the printer Roller Assembly, (ON, OFF, TURNING)
* Support the bumper accelerator
* Support the heads assemblies with all the signals needed for the printing mechanism
* Control the printed data flow and timing during printing

# Applicable Documents

# Summary of Accessible Registers

Table 1- OHDB Registers

| 1. Address | 1. Read/ | 1. Data Arrangement | | | | | | | | | | | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 1. Write | 1. D15 | 1. D14 | 1. D13 | 1. D12 | | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | | 1. D0 |
| 0x01 | W | Start Peg | | | | | | | | | | | | | | | | | |
| 0x01 | R | Actual Position | | | | | | | | | | | | | | | | | |
| 0x02 | R/W | End Peg | | | | | | | | | | | | | | | | | |
| 0x03 | R/W |  | | | | | | | | | GO Control | | | | | | | | |
| 0x04 | R/W |  | | | | Diagnostics | | | | | | | | | | | | | |
| 0x05 | R |  | | | | | | | | | | | | | FIFO Status | | | | |
| 0x06 | W |  | | | | | Heaters Control | | | | | | | | | | | | |
| 0x08 | R |  | | | | | | | | | FPGA Version | | | | | | | | |
| 0x09 | R |  | | | | | | | | | Board Revision | | | | | | | | |
| 0x09 | W |  | | | | | | | | | Roller Control | | | | | | | | |
| 0x0A | R/W | Roller Steps Divider | | | | | | | | | | | | | | | | | |
| 0x0B | W | Bumper End Peg | | | | | | | | | | | | | | | | | |
| 0x0C | W | Bumper Start Peg | | | | | | | | | | | | | | | | | |
| 0x10 | W |  | | | | | | | | | | | | | | | | Reset All | |
| 0x11 | W | Reset State Machines | | | | | | | | | | | | | | | | 🡨 Machines | |
| 0x1A | R/W | Strobe Delay | | | | | | | | | | | | | | | | | |
| 0x1B | R/W | Strobe Width | | | | | | | | | | | | | | | | | |
| 0x1D | W | Pulser operating Mode | | | | | | | | | | | | | | | | 🡨 | |
| 0x1E | W | Vpp Mux Control | | | | | | | | | | | | | | | | 🡨 | |
| 0x20 | R/W |  | | | | | | | | | | | | | Data Multiplier | | | | |
| 0x21 | R/W |  | | | | | | | | | | | | | Resolution Devider | | | | |
| 0x2A | W |  | | | | | | | | | Packets Loading to FIFO in JS mode | | | | | | | | |
| 0x2B | W | FIFO Data Source | | | | | | | | | | | | | | | | 🡨 | |
| 0x30 | R |  | | | | | | | | | Bumper Impact | | | | | | | | |
| 0x31 | W |  | | | | | | | | | Head’s firing mask | | | | | | | | |
| 0x32 | R | Read Home Position | | | | | | | | | | | | | | | | 🡨 | |
| 0x35 | R/W | Encoder Simulator Fire Frequency | | | | | | | | | | | | | | | | | |
| 0x37 | R/W | Number Of Fires – ON Duty Cycle (MSB) (Diag Mode) | | | | | | | | | | | | | | | | | |
| 0x38 | R/W | Number Of Fires – ON Duty Cycle (LSB) (Diag Mode) | | | | | | | | | | | | | | | | | |
| 0x39 | R/W | Number Of Fires – OFF Duty Cycle (MSB) (Diag Mode) | | | | | | | | | | | | | | | | | |
| 0x3A | R/W | Number Of Fires – OFF Duty Cycle (LSB) (Diag Mode) | | | | | | | | | | | | | | | | | |
| 0x3B | R/W | Number Of Cycles (Diag Mode) | | | | | | | | | | | | | | | | | |
| 0x40 | R/W | Number Of Fires in Travel | | | | | | | | | | | | | | | | | |
| 0x60 | R/W |  | | | Heaters Enable | | | | | | | | | | | | | | |
| 0x68 | W | Heaters Disable/Enable | | | | | | | | | | | | | | | | 🡨 | |
| 0x70 | W | LVDS Comm Enable | | | | | | | | | | | | | | | 🡨 | | |
| 0x76 | W | Bumper PEG Bypass | | | | | | | | | | | | | | | 🡨 | | |
| 0x80 | R | Encoder pulse counter | | | | | | | | | | | | | | | | | |
| 0x90 | R/W |  | | | | | | Fans on/off operation | | |  | | | | | | | | |
| 0x92 | W |  | | | | | | | | | Fans Speed Control | | | | | | | | |
| 0x93 | W |  | | | | | | | | | | | | | LIN to HIN Pulser Delay | | | | |
| 0x94 | W |  | | | | | | | | | | | | | Dynamic Active Nuzzles Counter | | | | |
| 0x95 | W |  | | | | | | | | | MN to LIN Pulser Signal Delay | | | | | | | | |
| 0x96 | W |  | | | | | | | | | HIN Pulser Signal to MN Delay | | | | | | | | |
| 0xA0 | R |  | | | | | | | | | Reset Status | | | | | | | | |
| 0xA1 | W | External Pump on/off Control | | | | | | | | | | | | | | | | | 🡨 |
| 0xA2 | R | External Pump Status | | | | | | | | | | | | | | | | | 🡨 |
| 0xA5 | R/W |  | | | | | | | | | | | | | Power Reset | | | | |
| 0xB0 | R/W |  | | | | | | | | | Head #1 Pulse1 F.T. | | | | | | | | |
| 0xB1 | R/W |  | | | | | | | | | Head #2 Pulse1 F.T. | | | | | | | | |
| 0xB2 | R/W |  | | | | | | | | | Head #3 Pulse1 F.T. | | | | | | | | |
| 0xB3 | R/W |  | | | | | | | | | Head #4 Pulse1 F.T. | | | | | | | | |
| 0xB4 | R/W |  | | | | | | | | | Head #5 Pulse1 F.T. | | | | | | | | |
| 0xB5 | R/W |  | | | | | | | | | Head #6 Pulse1 F.T. | | | | | | | | |
| 0xB6 | R/W |  | | | | | | | | | Head #7 Pulse1 F.T. | | | | | | | | |
| 0xB7 | R/W |  | | | | | | | | | Head #8 Pulse1 F.T. | | | | | | | | |
| 0xB8 | R/W |  | | | | | | | | | Head #1 Pulse2 Width | | | | | | | | |
| 0xB9 | R/W |  | | | | | | | | | Head #2 Pulse2 Width | | | | | | | | |
| 0xBA | R/W |  | | | | | | | | | Head #3 Pulse2 Width | | | | | | | | |
| 0xBB | R/W |  | | | | | | | | | Head #4 Pulse2 Width | | | | | | | | |
| 0xBC | R/W |  | | | | | | | | | Head #5 Pulse2 Width | | | | | | | | |
| 0xBD | R/W |  | | | | | | | | | Head #6 Pulse2 Width | | | | | | | | |
| 0xBE | R/W |  | | | | | | | | | Head #7 Pulse2 Width | | | | | | | | |
| 0xBF | R/W |  | | | | | | | | | Head #8 Pulse2 Width | | | | | | | | |
| 0xC0 | R/W |  | | | | | | | | | Head #1 Pulse1 Dwell Time | | | | | | | | |
| 0xC1 | R/W |  | | | | | | | | | Head #2 Pulse1 Dwell Time | | | | | | | | |
| 0xC2 | R/W |  | | | | | | | | | Head #3 Pulse1 Dwell Time | | | | | | | | |
| 0xC3 | R/W |  | | | | | | | | | Head #4 Pulse1 Dwell Time | | | | | | | | |
| 0xC4 | R/W |  | | | | | | | | | Head #5 Pulse1 Dwell Time | | | | | | | | |
| 0xC5 | R/W |  | | | | | | | | | Head #6 Pulse1 Dwell Time | | | | | | | | |
| 0xC6 | R/W |  | | | | | | | | | Head #7 Pulse1 Dwell Time | | | | | | | | |
| 0xC7 | R/W |  | | | | | | | | | Head #8 Pulse1 Dwell Time | | | | | | | | |
| 0xD0 | R/W |  | | | | | | | | | Head #1 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xD1 | R/W |  | | | | | | | | | Head #2 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xD2 | R/W |  | | | | | | | | | Head #3 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xD3 | R/W |  | | | | | | | | | Head #4 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xD4 | R/W |  | | | | | | | | | Head #5 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xD5 | R/W |  | | | | | | | | | Head #6 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xD6 | R/W |  | | | | | | | | | Head #7 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xD7 | R/W |  | | | | | | | | | Head #8 pulse1 to Pulse2 Delay (Double Pulse Mode) | | | | | | | | |
| 0xDA | R | FIFO Writes Counter | | | | | | | | | | | | | | | | | |
| 0xDB | R | FIFO Reads Counter | | | | | | | | | | | | | | | | | |
| 0xF0 | R | Status | | | | | | | | | | | | | | | | | |

## Detailed Register Descriptions

## Start Peg Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| Start Peg | | | | | | | | | | | | | | | |
| 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x01 | | | |
| Description | | This register is used for defining the encoder counter value from which the hardware starts firing data through the nozzles when the encoder counter counts up (when printing head is moving forword) | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | Start Peg | |  | X | 0x00 |

## Actual Position Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| Actual Position | | | | | | | | | | | | | | | |
| 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x01 | | | |
| Description | | This register holds the current value of the encoder pulses counter | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | Actual Position | | X |  | 0x00 |

## End Peg Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| End Peg | | | | | | | | | | | | | | | |
| 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x02 | | | |
| Description | | This register is used for defining the encoder counter value from which the hardware starts firing data through the nozzles when the encoder counter counts down (when printing head is moving backword) | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | End Peg | |  | X | 0x00 |

## Control Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | GO | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. R/W | |
| Address | | | | 0x03 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used for controlling printing mechanism | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | GO: Is used by the hardware to enable the printing mechanism  0: Disable printing  1: Enable printing | | | | | | | | | | | | | X | | X | | 0x0 | |

## Diagnostics Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D12 | | 1. D11 | 1. D10 | | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | | 1. D1 | | 1. D0 | |
| 1. STROBE 2. On/Off | | 1. Not 2. Used | 1. ROLLER SPD NOT OK | | 1. EOD 2. BYPASS | 1. FIFO 2. EMPTY | 1. Not 2. Used | 1. Not 2. Used | 1. CONT. 2. FIRE | 1. V. ENC 2. DIR | 1. OR With DATA\_IN | 1. Not 2. Used | | | 1. HOME SIM | | 1. ENC SIM | |
| 1. R/W | | 1. R/W | 1. R/W | | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | | | 1. R/W | | 1. R/W | |
| Address | | | | 0x04 | | | | | | | | | | | | | |
| Description | | | | This register is used for activating the hardware in diagnostics mode to enable testing of the on board mechanisms | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | |
| 1. Bit | 1. Description | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0 | ENC SIMULATOR: Is used by the hardware to enable simulation of encoder pulses  0: No Simulation  1: Encoder Simulated | | | | | | | | | | | | X | X | | 0x0 | |
| 1 | HOME SIMULATOR: Is used by hardware to enable the Home position indicator  0: No Simulation  1: Home position indicator signal is simulated by hardware | | | | | | | | | | | | X | X | | 0x0 | |
| 2 | Not Used | | | | | | | | | | | | X | X | | 0x0 | |
| 3 | OR With DATA\_IN:  0: output data = DATA\_IN  1: output data = ‘1’ (all nuzzles are on regardless data) | | | | | | | | | | | | X | X | | 0x0 | |
| 4 | Synthetic Encoder Direction  0: Left  1: Right | | | | | | | | | | | | X | X | | 0x0 | |
| 5 | CONTINOUS FIRE  0: No Action  1: Continous fire  This bit works in conjuction with bits D0 –D3 and with the GO bit to force continous firing of data | | | | | | | | | | | | X | X | | 0x0 | |
| 6 | Not Used | | | | | | | | | | | | X | X | | 0x0 | |
| 7 | Not Used | | | | | | | | | | | | X | X | | 0x0 | |
| 8 | FIFO Empty Simulation  0: Simulate FIFO empty off  1: Simulate FIFO empty on | | | | | | | | | | | | X | X | | 0x0 | |
| 9 | End Of Data (EOD) bypass  0: State machine is depanding of EOD signal to continue  1: Bypass EOD signal (endless firing regardless FIFO state) | | | | | | | | | | | | X | X | | 0x0 | |
| 10 | Roller Speed Not OK bypass  0: Speed Not Ok signal enabled  1: Bypass roller speed not ok signal | | | | | | | | | | | | X | X | | 0x0 | |
| 11 | Not Used | | | | | | | | | | | | X | X | | 0x0 | |
| 12 | Strobe Mechanism On/Off (Jetting Station)  0: Strobe is off  1: Strobe is on | | | | | | | | | | | | X | X | | 0x0 | |

## FIFO Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  | FULL | | EMPTY | | AF | | AE | |
|  |  | |  | |  |  |  |  |  |  |  |  |  | 1. R | | 1. R | | 1. R | | 1. R | |
| Address | | | | 0x05 | | | | | | | | | | | | | | | | |
| Description | | | | This register gives status of the main FIFO. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | Almost Empty signal | | | | | | | | | | | | | X | |  | | 0x0 | |
| 1 | | Almost Full signal | | | | | | | | | | | | | X | |  | | 0x0 | |
| 2 | | FIFO empty signal | | | | | | | | | | | | | X | |  | | 0x1 | |
| 3 | | FIFO full signal | | | | | | | | | | | | | X | |  | | 0x0 | |

## Heater Timer Control Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. W | |
| Address | | | | 0x06 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used for resetting heaters timer. If after 2 seconds this register sin’t activated, a heaters are disabled. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | Heater timer control  0: Heaters timer is OFF  1: Heaters timer is ON | | | | | | | | | | | | |  | | X | | 0x0 | |

## FPGA Version

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R |

Address 0x08

Description FPGA Firmware version

## Board Revision

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  | 1. R | 1. R | 1. R | 1. R |

Address 0x09

Description Board revision

## Roller Control Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | | 1. W | | 1. W | |
| Address | | | | 0x09 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used for controlling the Roller mechanisms. For normal operation both “ROLLER ON/OFF” and  “ENABLE ROLLER DRIVER” bits should be set to “1” | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | ROLLER ON/OFF: Turns Roller mechanism On or Off  0: Roller Off  1: Roller On | | | | | | | | | | | | | X | | X | | 0x0 | |
| 1 | | ENABLE ROLLER DRIVER: Enables the Roller Motor driver  0: Driver is disabled  1: Driver is enabled | | | | | | | | | | | | | X | | X | | 0x0 | |

## Roller Steps Divider Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| STEPS DIVIDER | | | | | | | | | | | | | | | |
| 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x0A | | | |
| Description | | This register is used for initializing and controlling hardware mechanisms | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | STEPS DIVIDER: | |  | X | 0x0 |

## Bumper End Peg Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| BUMPER END PEG | | | | | | | | | | | | | | | |
| 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x0B | | | |
| Description | | This register is used for defining the encoder counter value from which the hardware starts or stops responding to bumper signals depending on the movement direction. Counter values above this value disable bumper detection Counter values beneath this value and above the  “BUMPER START PEG” value enable bumper detection. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | BUMPER END PEG | |  | X | 0x00 |

## Bumper Start Peg Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| BUMPER START PEG | | | | | | | | | | | | | | | |
| 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x0C | | | |
| Description | | This register is used for defining the encoder counter value from which the hardware starts or stops responding to bumper signals depending on the movement direction. Counter values above this value and beneath the “BUMPER END PEG” value enable bumper detection. Counter values beneath this value disable bumper detection. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | BUMPER START PEG | |  | X | 0x00 |

## Reset All

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. W | |
| Address | | | | 0x10 | | | | | | | | | | | | | | | | |
| Description | | | | Resetting all state machines and registers to default values. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | Reset All | | | | | | | | | | | | |  | | X | | 0x00 | |

## Reset State Machines

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
| 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x11 | | | |
| Description | | Reset state machines without resetting registers to their default values. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0 | Reset State Machine | |  | X | 0x0 |

## Strobe Delay

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x1A | | | |
| Description | | This register is used for defining the delay between fire pulse and strobe pulse, in jetting station. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | Strobe pulse delay | | X | X | 0x0 |

## Strobe Pulse Width

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x1B | | | |
| Description | | This register is used for defining the strobe pulse width in jetting station | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | Strobe pulse width | | X | X | 0x0 |

## Pulser Operating Mode

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | X |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x1D | | | |
| Description | | This register is used for defining the pulser operating mode – single pulse or double pulse. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0 | Pulser opearing mode:  0: Single Pulse  1: Double Pulse | |  | X | 0x0 |

## Head5 Delay Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. W | |
| Address | | | | 0x1E | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to control Vpp mux in head drive board. Because of lack of analog sensing signal, we multiplex two Vpp sensing on single line | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | Vpp mux control:  0: Odd head Vpp reading  1: Even head Vpp reading | | | | | | | | | | | | |  | | X | | 0x0 | |

## Data Multiplier

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  | 1. R/W | | 1. R/W | | 1. R/W | | 1. R/W | |
| Address | | | | 0x20 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to control how many times the data uploaded to head will be used before uploading new data from FIFO. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-3 | | Data multiplication | | | | | | | | | | | | | X | | X | | 0x0 | |

## Resoulotion Devider Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  | 1. R/W | | 1. R/W | | 1. R/W | | 1. R/W | |
| Address | | | | 0x21 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to define the divider that divides the basic encoder resolution (4800dpi) | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-7 | | HEAD DELAY: | | | | | | | | | | | | | X | | X | | 0x4 | |

## Packets Loading from RS-232 CS (Jetting Station)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  | 1. W | 1. W | 1. W | 1. W | 1. W | | 1. W | | 1. W | | 1. W | |
| Address | | | | 0x2A | | | | | | | | | | | | | | | | |
| Description | | | | On every CS signal a 8bit data is loading to FIFO data register. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-7 | | Data from RS-232 in Jetting station mode | | | | | | | | | | | | |  | | X | | 0x0 | |

## FIFO Data Source

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. W | |
| Address | | | | 0x2B | | | | | | | | | | | | | | | | |
| Description | | | | This register defines the data source which the FIFO will be loaded. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | FIFO Data Source:  0: DATA-PCI  1: RS-232 | | | | | | | | | | | | |  | | X | | 0x0 | |

## Bumper Impact Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | | |  | | IMPACT | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | | |  | | 1. R | |
| Address | | | | 0x30 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used for reading the status of the impact detection mechanism. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0 | | IMPACT:  0: No impact was detected since last read  1: Impact was detected since last read  Hardwre reset resets this status bit to “0” | | | | | | | | | | | | | | X |  | | 0x0 | |

## Heads Firing Mask

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x31 | | | |
| Description | | This register is used for masking head’s firing. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0 | Head #1 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |
| 1 | Head #2 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |
| 2 | Head #3 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |
| 3 | Head #4 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |
| 4 | Head #5 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |
| 5 | Head #6 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |
| 6 | Head #7 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |
| 7 | Head #8 mask:  0: Head fire enable  1: Head fire disable | |  | X | 0x0 |

## Home Position

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. R | |
| Address | | | | 0x32 | | | | | | | | | | | | | | | | |
| Description | | | | Reads home position signal. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | 0: Not in home position  1: Block is in home position | | | | | | | | | | | | | X | |  | | 0x0 | |

## Encoder Simulator Fire Frequency Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| SIMULATOR FIRE FREQUENCY VALUE | | | | | | | | | | | | | | | |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x35 | | | |
| Description | | This register is used for setting the fire frequency for simulation mode | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | SIMULATOR FIRE FREQUENCY VALUE:  SIMULATOR FIRE FREQUENCY VALUE = 33.333Mhz / (4 \* DesiredFireFrequency)  Accepted Values of “Required Frequencies” can be calculated by RequiredFrwquency = 33333333 Hz / (4 \* SIMULATOR FIRE FREQUENCY VALUE)  Min Val = 127.158 Hz  Max Val =8333333 Hz | | X | X | 0x0 |

## Number Of Fires – D.C. ON (MSB)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| NUMBER OF FIRES ON (MSB) | | | | | | | | | | | | | | | |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x37 | | | |
| Description | | This register is used for defining the number of fire pulses to output as part of firing in duty cycle. This register contain the 16bit MSB data of 32bit ON register | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | 16bit MSB of 32bit register of number of fires for ON duty-cycle | | X | X | 0x0 |

## Number Of Fires – D.C. ON (LSB)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| NUMBER OF FIRES ON (LSB) | | | | | | | | | | | | | | | |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x38 | | | |
| Description | | This register is used for defining the number of fire pulses to output as part of firing in duty cycle. This register contain the 16bit LSB data of 32bit ON register | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | 16bit LSB of 32bit register of number of fires for ON duty-cycle | | X | X | 0x0 |

## Number Of Fires – D.C. OFF (MSB)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| NUMBER OF FIRES OFF (MSB) | | | | | | | | | | | | | | | |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x39 | | | |
| Description | | This register is used for defining the number of fire pulses to output as part of firing in duty cycle. This register contain the 16bit MSB data of 32bit OFF register | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | 16bit MSB of 32bit register of number of fires for OFF duty-cycle | | X | X | 0x0 |

## Number Of Fires – D.C. OFF (LSB)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| NUMBER OF FIRES OFF (LSB) | | | | | | | | | | | | | | | |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x3A | | | |
| Description | | This register is used for defining the number of fire pulses to output as part of firing in duty cycle. This register contain the 16bit LSB data of 32bit OFF register | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | 16bit LSB of 32bit register of number of fires for OFF duty-cycle | | X | X | 0x0 |

## Number Of Cycles

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| NUMBER OF CYCLES | | | | | | | | | | | | | | | |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x3B | | | |
| Description | | This register is used for defining the number of fire cycles | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | Number of fires cycle to do in simulation mode. | | X | X | 0x0 |

## Number Of Fires In Travel

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| NUMBER OF FIRES IN TRAVEL | | | | | | | | | | | | | | | |
| 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x40 | | | |
| Description | | This register is used to control the number of fires needed in each block travel. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | Number of fires in travel. | | X | X | 0x0 |

## Heaters On/Off Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  | PRE | BLK4 | BLK3 | BLK2 | BLK1 | HD8 | HD7 | HD6 | HD5 | HD4 | HD3 | HD2 | HD1 |
|  |  |  | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x60 | | | |
| Description | | This register is used for controlling heads & block heaters on and off. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0 | Head #1 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 1 | Head #2 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 2 | Head #3 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 3 | Head #4 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 4 | Head #5 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 5 | Head #6 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 6 | Head #7 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 7 | Head #8 heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 8 | Block heater #1 control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 9 | Block heater #2 control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 10 | Block heater #3 control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 11 | Block heater #4 control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |
| 12 | Block pre-heater control:  0: Heater off.  1: Heater on. | | X | X | 0x0 |

## All Heaters Disable/Enable

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EN/DIS |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x68 | | | |
| Description | | This register is used for enable/disable all heaters at once. To use register 0x60 – “Heaters On/Off Control” this register should be ‘1’ at D0. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0 | Enable/Disable all heaters | |  | X | 0x0 |

## LVDS (Data-PCI) Communication Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  | DATA | CLK |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x70 | | | |
| Description | | This register is used to enable/disable the communication between Data-PCI and OHDB. It controls the clock and serial data signals that come from Data-PCI board. | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0 | Enable/Disable LVDS clock signal | |  | X | 0x0 |
| 1 | Enable/Disable LVDS serial data signal | |  | X | 0x0 |

## Bumper PEG Bypass

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  | BMPR2 | BMPR1 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1. W | 1. W |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x76 | | | |
| Description | | This register is used to bypass bumper PEG area. It used to check bumper signal outside PEG area | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0 | Bypass main bumper signal  0: Bypass is off  1: Bypass is on | |  | X | 0x0 |
| 1 | Bypass secondary bumper signal  0: Bypass is off  1: Bypass is on | |  | X | 0x0 |

## Encoder Pulses Counter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | 1. D13 | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | 1. D1 | 1. D0 |
| ENCODER PULSES COUTER | | | | | | | | | | | | | | | |
| 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address | | 0x80 | | | |
| Description | | This register is used to read encoder pulses counter. This is used to determine block position | | | |
| Reset Value | |  | | | |
| 1. Bit | 1. Description | | 1. Read | 1. Write | 1. Reset Value |
| 0-15 | Encoder pulses counter | | X |  | 0x0 |

## Material Fans Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  | M | L | R |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  | 1. W | 1. W | 1. W |  |  |  |  |  | |  | |  | |  | |
| Address | | | | 0x90 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to read encoder pulses counter. This is used to determine block position | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 8 | | Material right fan control:  0: Off  1: On | | | | | | | | | | | | | X | | X | | 0x0 | |
| 9 | | Material left fan control:  0: Off  1: On | | | | | | | | | | | | | X | | X | | 0x0 | |
| 10 | | Material middle fan control:  0: Off  1: On | | | | | | | | | | | | | X | | X | | 0x0 | |

## Material Fans Speed Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  | 1. W | 1. W | 1. W | 1. W | 1. W | | 1. W | | 1. W | | 1. W | |
| Address | | | | 0x92 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to control the material fans speed. The value is the “ON” period as part of a duty cycle of 256kHz clock period | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-7 | | Material fans speed value. | | | | | | | | | | | | |  | | X | | 0xFF | |

## LIN to HIN Pulser Signals Delay

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  | 1. W | | 1. W | | 1. W | | 1. W | |
| Address | | | | 0x93 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to determine the delay between the LIN and HIN digital signals that control the power-mosfets transistors of VCOM analog fire pulse | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-3 | | LIN to HIN digital signals delay | | | | | | | | | | | | |  | | X | | 0x05 | |

## Dynamic Active Nuzzles Counter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  | 1. W | | 1. W | | 1. W | | 1. W | |
| Address | | | | 0x94 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to store the divider of the number of active nuzzles upload to head in current fire. Every division with this number, a one system clock period (30nsec) is added to first pulse F.T counter in double pulse mode. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-3 | | Divider of the sum of active nuzzles in current fire | | | | | | | | | | | | |  | | X | | 0x05 | |

## MN to LIN Pulser Signals Delay

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  | 1. W | 1. W | 1. W | 1. W | 1. W | | 1. W | | 1. W | | 1. W | |
| Address | | | | 0x95 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to determine the delay between the MN and LIN digital signals. The counts are in clock of 30nsec.  MN control signal needs to be enabled before start of pulse. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-7 | | MN to LIN digital signals delay | | | | | | | | | | | | |  | | X | | 0x20 | |

## HIN to MN Pulser Signals Delay

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  | 1. W | 1. W | 1. W | 1. W | 1. W | | 1. W | | 1. W | | 1. W | |
| Address | | | | 0x96 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to determine the delay between the HIN and MN digital signals. The counts are in clock of 30nsec.  MN control signal needs to be disabled after end of pulse. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-7 | | HIN to MN digital signals delay | | | | | | | | | | | | |  | | X | | 0x96 | |

## Reset Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  | 1. R | 1. R | 1. R | 1. R | 1. R | | 1. R | | 1. R | | 1. R | |
| Address | | | | 0xA0 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to read the number of resets done from power-up. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0-7 | | Reset status counter | | | | | | | | | | | | | X | |  | | 0x0 | |

## External Pump On/Off Control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. W | |
| Address | | | | 0xA1 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to enable/disable external pump. This signal goes to step-motor board. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | External pump control  0: Pump off.  1: Pump on. | | | | | | | | | | | | |  | | X | | 0x0 | |

## External Pump Status

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | | 1. D2 | | 1. D1 | | 1. D0 | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | |  | |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  | |  | |  | | 1. R | |
| Address | | | | 0xA2 | | | | | | | | | | | | | | | | |
| Description | | | | This register is used to read external pump status. | | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | | 1. Write | | 1. Reset Value | |
| 0 | | External pump status  0: Pump off.  1: Pump on. | | | | | | | | | | | | | X | |  | | 0x0 | |

## Pulse1 F.T

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | 1. D1 | | 1. D0 |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | |  | |  |
|  |  | |  | |  |  |  |  |  | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | | 1. R/W | | 1. R/W |
| Address | | | | 0xB0 – 0xB7 | | | | | | | | | | | | | | | |
| Description | | | | These registers use FPGA system clock (30nsec) to count the F.T of pulse in single pulse mode or first pulse in double pulse mode.  Address range are for head #1 to head #8 respectively | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0-7 | | Pulse1 F.T in single and double pulse mode | | | | | | | | | | | | | X | X | | 0x00 | |

## Pulse2 Width

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | 1. D1 | | 1. D0 |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | |  | |  |
|  |  | |  | |  |  |  |  |  | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | | 1. R/W | | 1. R/W |
| Address | | | | 0xB8 – 0xBF | | | | | | | | | | | | | | | |
| Description | | | | These registers use FPGA system clock (30nsec) to count the width of second pulse in double pulse mode.  Address range are for head #1 to head #8 respectively | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0-7 | | Pulse2 width in double pulse mode | | | | | | | | | | | | | X | X | | 0x00 | |

## Pulse1 Dwell Time

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | 1. D1 | | 1. D0 |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | |  | |  |
|  |  | |  | |  |  |  |  |  | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | | 1. R/W | | 1. R/W |
| Address | | | | 0xC0 – 0xC7 | | | | | | | | | | | | | | | |
| Description | | | | These registers use FPGA system clock (30nsec) to count the dwell time of first pulse in double pulse mode.  Address range are for head #1 to head #8 respectively | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0-7 | | Pulse1 dwell time in double pulse mode | | | | | | | | | | | | | X | X | | 0x00 | |

## Pulse1 to Pulse2 Delay

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | 1. D1 | | 1. D0 |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | |  | |  |
|  |  | |  | |  |  |  |  |  | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | 1. R/W | | 1. R/W | | 1. R/W |
| Address | | | | 0xD0 – 0xD7 | | | | | | | | | | | | | | | |
| Description | | | | These registers use FPGA system clock (30nsec) to count delay time between start of pulse1 rising to start of pulse2 falling edge in double pulse mode.  Address range are for head #1 to head #8 respectively | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0-7 | | Pulse1 to pulse2 delay in double pulse mode | | | | | | | | | | | | | X | X | | 0x00 | |

## FIFO Writes Counter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | 1. D1 | | 1. D0 |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | |  | |  |
| 1. R | 1. R | | 1. R | | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | | 1. R | | 1. R |
| Address | | | | 0xDA | | | | | | | | | | | | | | | |
| Description | | | | This register is used to read number of words written to FIFO. | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0-15 | | Number of words written to FIFO | | | | | | | | | | | | | X |  | | 0x00 | |

## FIFO Reads Counter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | 1. D1 | | 1. D0 |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | |  | |  |
| 1. R | 1. R | | 1. R | | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | | 1. R | | 1. R |
| Address | | | | 0xDB | | | | | | | | | | | | | | | |
| Description | | | | This register is used to read number of words read from FIFO. | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0-15 | | Number of words read from FIFO | | | | | | | | | | | | | X |  | | 0x00 | |

## Status Register

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. D15 | 1. D14 | | 1. D13 | | 1. D12 | 1. D11 | 1. D10 | 1. D9 | 1. D8 | 1. D7 | 1. D6 | 1. D5 | 1. D4 | 1. D3 | 1. D2 | | 1. D1 | | 1. D0 |
|  |  | |  | |  |  |  |  |  |  |  |  |  |  |  | |  | |  |
| 1. R | 1. R | | 1. R | | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | 1. R | | 1. R | | 1. R |
| Address | | | | 0xF0 | | | | | | | | | | | | | | | |
| Description | | | | This register contain status bits | | | | | | | | | | | | | | | |
| Reset Value | | | |  | | | | | | | | | | | | | | | |
| 1. Bit | | 1. Description | | | | | | | | | | | | | 1. Read | 1. Write | | 1. Reset Value | |
| 0-15 | | TBD | | | | | | | | | | | | | X |  | | 0x00 | |